Electronic Version
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Claims

[c1] 1. A method for operating a dual pumping circuit comprising at least one stage, each stage comprising a first pumping unit and a second pumping unit mirrored to the first pumping unit, the first pumping unit comprising;

a main pass transistor with gate, source, and drain terminals and a body, each main pass transistor of each stage being connected in series with main pass transistors of a preceding and a subsequent stage, and the body of the main pass transistor being electrically coupled to a main pass transistor of the second pumping unit;

a boosting transistor with gate, source, and drain terminals and a body, the drain terminal of the boosting transistor being electrically coupled to the gate terminal of the main pass transistor, the source of the boosting transistor being electrically coupled to the drain of the main pass transistor, and the gate of the boosting transistor being electrically coupled to the source of the main pass transistor;

a substrate transistor with gate, source, and drain terminals and a body, the gate terminal of the substrate tran-

sistor being electrically coupled to the source terminal of the boosting transistor, the drain terminal of the main pass transistor, and the source of a substrate transistor of the second pumping unit, the drain terminal of the substrate transistor being electrically coupled to the bodies of the main pass transistor and the boosting transistor, the source terminal of the substrate transistor being electrically coupled to a gate terminal of a substrate transistor and a drain terminal of a main pass transistor and a source terminal of a boosting transistor of the second pumping unit, and the body of the substrate transistor being electrically coupled to a main pass transistor in the subsequent stage;

two small charge storing devices respectively electrically coupled to the gate of the main pass transistor of the first pumping unit and the second pumping unit; and

two large charge storing devices respectively electrically coupled to the drains of the main pass transistors of the first pumping unit and the second pumping unit;

the method for the first stage of the dual pumping circuit comprising:

supplying an input voltage to the source terminals of the main pass transistors of the first pumping unit and the second pumping unit;

in interval one, rendering the main pass transistor of the second pumping unit, the substrate transistor of the

second pumping unit, and the boosting transistors of the first pumping unit and the main pass transistor of the first pumping unit off, and the substrate transistor of the first pumping unit and the boosting transistor of the second pumping unit on;

in interval two, rendering the main pass transistor of the first pumping unit, the substrate transistor of the first pumping unit, and the boosting transistor of the second pumping unit on, and the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off;

in interval three, rendering the main pass transistor of the first pumping unit, the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off, the boosting transistor of the second pumping unit, and the substrate transistor of the first pumping unit on;

in interval four, rendering the substrate transistor of first pumping unit, the main pass transistor of the first pumping unit, the main pass transistor of the second pumping unit, and the boosting transistor of the second pumping unit off, the boosting transistor of the first pumping unit and the substrate transistor of the second pumping unit on;

in interval five, rendering the main pass transistor of the second pumping unit, the substrate transistor of the second pumping unit, and the boosting transistor of the first pumping unit on, and the substrate transistor of the first pumping unit, the main pass transistor of the first pumping unit, and the boosting transistor of the second pumping unit off; and

in interval six, rendering the main pass transistor of the second pumping unit, the substrate transistor of the first pumping unit, the main pass transistor of the first pumping unit, and the boosting transistor of the second pumping unit off, and the substrate transistor of the second pumping unit and the boosting transistor of the first pumping unit on.

[c2] 2. The method in claim 1 for each even stage of the dual pumping circuit comprising:

in interval one, rendering the substrate transistor of the first pumping unit and the boosting transistor of the second pumping unit on, the main pass transistor of the first pumping unit, the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off;

in interval two, rendering the main pass transistor of the first pumping unit, the substrate transistor of the first

pumping unit, and the boosting transistor of the second pumping unit on, and the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off;

in interval three, rendering the substrate transistor of the first pumping unit and the boosting transistor of the second pumping unit on, and the main pass transistor of the first pumping unit, the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit being kept off;

in interval four, rendering the substrate transistor of first pumping unit, the boosting transistor of the second pumping unit, the main pass transistor of the first pumping unit, and the main pass transistor of the second pumping unit off, the substrate transistor of the second pumping unit and the boosting transistor of the first pumping unit on;

in interval five, rendering the substrate transistor of first pumping unit, the boosting transistor of the second pumping unit, and the main pass transistor of the first pumping unit off, the substrate transistor of the second pumping unit, the boosting transistor of the first pumping unit, and the main pass transistor of the second pumping unit on; and

in interval six, rendering the substrate transistor of first pumping unit, the boosting transistor of the second pumping unit, the main pass transistor of the first pumping unit, and the main pass transistor of the second pumping unit off, and the substrate transistor of the second pumping unit and the boosting transistor of the first pumping unit on.

[c3] 3. The method in claim 2 for each odd stage of the dual pumping circuit except the first stage comprising:
in interval one, rendering the substrate transistor of first pumping unit, the boosting transistor of the second pumping unit, the main pass transistor of the first pumping unit, and the main pass transistor of the second pumping unit off, and the substrate transistor of the second pumping unit and the boosting transistor of the first pumping unit on;
in interval two, rendering the substrate transistor of first pumping unit, the boosting transistor of the second pumping unit, and the main pass transistor of the first pumping unit off, the substrate transistor of the second pumping unit, the boosting transistor of the first pumping unit, and the main pass transistor of the second pumping unit on;
in interval three, rendering the substrate transistor of first pumping unit, the boosting transistor of the second

pumping unit, the main pass transistor of the first pumping unit, and the main pass transistor of the second pumping unit off, and the substrate transistor of the second pumping unit and the boosting transistor of the first pumping unit on;

in interval four, rendering the substrate transistor of the first pumping unit and the boosting transistor of the second pumping unit on, the main pass transistor of the first pumping unit, the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off;

in interval five, rendering the main pass transistor of the first pumping unit, the substrate transistor of the first pumping unit, and the boosting transistor of the second pumping unit on, the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off; and

in interval six, rendering the substrate transistor of the first pumping unit and the boosting transistor of the second pumping unit on, the main pass transistor of the first pumping unit, the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit being kept off.

[c4] 4. The method in claim 1, wherein the intervals one, two, three, four, five, and six are consecutive and in sequence.

[c5] 5. The method in claim 1, wherein the dual pumping circuit further comprising:
first and second output transistors each with source, drain, and gate terminals and a body, the first output transistor mirroring the second output transistor, the source terminal of the first output transistor being electrically coupled to the drain terminal of the main pass transistor of the first pumping unit in a last stage, the gate terminal of the first output transistor being electrically coupled to the drain terminal of the substrate transistor of the second pumping unit in the last stage, and the body of the first output transistor being electrically coupled to the drain terminal of the substrate transistor of the second pumping unit in the last stage; the method further comprising:
rendering the first output transistor on when the substrate transistor of the second pumping unit in the last stage is rendered on and rendering the second output transistor off when the substrate transistor of the first pumping unit of the last stage is rendered off.

[c6] 6. The method in claim 1, wherein supplying a voltage to

the sources of the main pass transistors of the first stage is controlled by an inverter.

[c7] 7. The method in claim 1, wherein the body of the main pass transistor of the first pumping unit and the body of the main pass transistor of the second pumping unit in each stage of the dual pumping circuit are preset to an appropriate bias voltage before pumping.

[c8] 8. The method in claim 7, wherein the additional input voltage is controlled by a transistor that is electrically coupled to a capacitor.

[c9] 9. A dual pumping circuit comprising at least one stage, each stage comprising a first pumping unit and a second pumping unit which are mirrored to each other and each first pumping unit comprising;
a main pass transistor with gate, source, and drain terminals and a body, each main pass transistor of each stage being connected in series with main pass transistors of a preceding and a subsequent stage, and the body of the main pass transistor being electrically coupled to a main pass transistor of the second pumping unit;
a boosting transistor with gate, source, and drain terminals and a body, the drain terminal of the boosting transistor being electrically coupled to the gate terminal of

the main pass transistor, the source of the boosting transistor being electrically coupled to the drain of the main pass transistor, and the gate of the boosting transistor being electrically coupled to the source of the main pass transistor;

a substrate transistor with gate, source, and drain terminals and a body, the gate terminal of the substrate transistor being electrically coupled to the source terminal of the boosting transistor, the drain terminal of the main pass transistor, and the source of a substrate transistor of the second pumping unit, the drain terminal of the substrate transistor being electrically coupled to the bodies of the main pass transistor and the boosting transistor, the source terminal of the substrate transistor being electrically coupled to a gate terminal of a substrate transistor and a drain terminal of a main pass transistor and a source terminal of a boosting transistor of the second pumping unit, and the body of the substrate transistor being electrically coupled to a main pass transistor in the subsequent stage;

two small charge storing devices respectively electrically coupled to the gate of the main pass transistor of the first pumping unit and the second pumping unit; and

two large charge storing devices respectively electrically coupled to the drain of the main pass transistor of the first pumping unit and the second pumping unit.

[c10] 10.The dual pumping circuit in claim 9 further comprises a diode that is electrically coupled to each of the small charge storing devices and the large charge storing devices.

[c11] 11.The dual pumping circuit in claim 9 wherein the gate terminal of the boosting transistor of the first and the second pumping units in the first stage is electrically coupled to a supply voltage, and the gate terminals of the boosting transistors of the first and the second pumping units in a stage other than the first stage is electrically coupled to the source terminals of the boosting transistors of the first and the second pumping units in the previous stage, respectively.

[c12] 12. The dual pumping circuit in claim 9 further comprising a high voltage circuit applying to the two small charge storing devices for increasing a voltage level of clock pulses.

[c13] 13. The method in claim 9, wherein the dual pumping circuit further comprises:
first and second output transistors each with source, drain, and gate terminals and a body, the first output transistor mirroring the second output transistor, the source terminal of the first output transistor being elec-

trically coupled to the drain terminal of the main pass transistor of the first pumping unit in a last stage and the gate terminal of the second output transistor, the gate terminal of the first output transistor being electrically coupled to the drain terminal of the main pass transistor of the second pumping unit in the last stage, and the body of the first output transistor being electrically coupled to the drain terminal of the substrate transistor of the second pumping unit in the last stage.

[c14] 14. The dual pumping circuit in claim 9, wherein the main pass transistor, the boosting transistor, and the substrate transistor are NMOSFETs for negative pumping.

[c15] 15. The dual pumping circuit in claim 9, wherein the main pass transistor, the boosting transistor, and the substrate transistor are PMOSFETs for positive pumping.

[c16] 16. The dual pumping circuit in claim 9, wherein a first clock pulse is sent to the gate of the first substrate transistor of the first pumping unit, a second clock pulse is sent to the gate of the main pass transistor of the first pumping unit, a third clock pulse is sent to the gate of the substrate transistor of the second pumping unit, and a fourth clock pulse is sent to the gate of the main pass transistor of the second pumping unit where the first and third clock pulses are out of phase and the second

clock pulse turns on the main pass transistor of the first pumping unit for a shorter time than the first clock pulse does; and the fourth clock pulse turns on the main pass transistor of the second pumping unit for a shorter time than the third clock pulse does.